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REVERSE CONDUCTION PROTECTION METHOD AND APPARATUS FOR A DUAL POWER SUPPLY DRIVER

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REVERSE CONDUCTION PROTECTION METHOD AND APPARATUS FOR A DUAL POWER SUPPLY DRIVER

FIELD OF THE INVENTION

[0001] The invention relates to integrated circuits with dual power supplies at different voltage levels.

BACKGROUND OF THE INVENTION

[0002] Integrated circuits typically operate with power supplies of 5 volts or less and often must drive signals of a particular voltage level on-chip or off-chip. Merely as an example, an integrated circuit pre-amplifier may have a plurality of driver circuits for driving signals off-chip. For instance, an eight bit preamplifier for driving eight signals off-chip might have eight driver circuits having an output stage like the output stage 100 shown in Figure 1 for driving an off-chip load 102 through an output pad 104 of the integrated circuit. Figure 1 shows only the output stage of the driver circuit in detail. The input signal source, V_{IN}, that is to be driven onto the load 102 is supplied to one input terminal of an operational amplifier 105.

[0003] In the output stage 100, an output transistor M17 has its source coupled to a voltage rail 113, in this case 5 volts, and its drain coupled to node 107. Its gate is coupled to the output of the operational amplifier 105. Transistor

M16 has its source coupled to the voltage rail 113, and its drain and gate coupled together to the gate of output transistor M17 and the output of the operational amplifier 105. Transistors M16 and M17 in this circuit are configured as a current mirror that essentially delivers current controlled by the operational amplifier 105 to the load. The input signal VIN is supplied to one input terminal of the operational amplifier and the other input terminal is coupled to the junction 110 of voltage divider 109 comprising resistors R0 and R1. Since an operational amplifier operates to drive the voltages at its two inputs to the same voltage, operational amplifier 105 drives the junction 110 between resistors R0 and R1 to VIN. The voltage at the output pad 104 is dependent on the input voltage, VIN, and the ratio of resistors R0 and R1. Specifically, with this configuration, the output voltage on pad 104 is ((R0 + R1)/R1)*VIN. The current through the load 102 is dictated by the voltage placed on pad 104 and the resistance, R_{ext}, of the load 102. This type of architecture is efficient in that it generates maximum output voltage because the only voltage drop from the rail is the V_{ds} of M17. So the output voltage can go to a maximum value of VCC – V_{dsM17}.

[0004] Transistor M15 has its current flow terminals (source and drain) coupled between the drain of output transistor M17 and the load 102. The source is coupled to the drain of transistor M17 at node 107 and the drain is coupled to the output node 104. A voltage divider 109 is coupled between the output node 104 and ground with the divided voltage supplied to the second input of the operational amplifier 105. Transistor M15 acts as a source follower at lower output voltages, preventing the Vds breakdown of transistor M17. At

higher output voltages, transistor M15 acts as a pass gate, whereby the output voltage on node 104 follows the voltage at node 107 between transistors M15 and M17. This driver circuit should produce a very good output voltage range of about 0 to 4.5 volts.

[0005] In a multi-bit preamplifier circuit, (8-bit, for example) a single, "selected" driver typically drives the load over the full output range (e.g., about 0-4.5 volts), while the seven remaining, "unselected" drivers only need to drive their external loads to very low voltages (e.g., 0-1.5 volts). In such conditions, most of the excess voltage from the various drivers is dropped inside the chip. For example, if the unselected loads are to be driven to only 1 volt, then V_{CC} (5 volts) – 1 volt = 4 volts will be dropped inside the chip for each of the 7 unselected drivers. With seven drivers dumping 4 volts each on-chip, power dissipation on-chip can be quite substantial.

[0006] In many situations, e.g., when such circuits are employed in battery-powered devices, such as cellular telephones, PDAs (Personal Digital Assistants), and portable digital audio or video recording and playing devices, it is particularly desirable to minimize wasted power.

SUMMARY OF THE INVENTION

[0007] The invention is a dual power supply driver with a protection circuit for eliminating wasted power dissipation by preventing reverse conduction through the lower voltage power supply driver when the higher voltage power supply driver is driving a higher voltage signal to the output. In one embodiment

of the invention, the protection circuit comprises a protection transistor interposed between the output transistor of the lower voltage power supply driver and the output node to which both power supplies are coupled. The protection transistor is turned off under control of a comparator to prevent reverse conduction through the output stage of the lower voltage power supply driver when a high voltage is present on the output node. Specifically, the comparator detects the voltage on the output node and turns off the protection transistor when that voltage exceeds a predetermined level.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 is a circuit diagram of an output stage of a driver circuit of the prior art.

[0009] Figure 2 is a schematic diagram of a two stage driver circuit.

[0010] Figure 3 is a schematic diagram of the demultiplexer for a two stage driver in accordance with the present invention.

[0011] Figure 4 is a circuit diagram of the output stage of the lower voltage driver of a dual driver circuit in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0012] One technique to reduce power dissipation on the chip involves providing a dual power supply comprising a first, higher voltage driver (e.g., 5 volts) and a second, lower voltage driver (e.g., 2.5 volts). When a particular pad (0, 1 ...7) is selected, the 5 volt power supply driver is turned on and the 2.5 volt

power supply driver is turned off for the selected pad . At the remaining, unselected pads, the 5 volt power supply drivers are turned off and the 2.5 volt power supply drivers are turned on at all unselected PADs. This two stage scheme substantially reduces the wasted power dissipation on the chip because a 2.5 volt supply driver instead of 5 volt supply driver can still provide 1 volt across the load, while dumping only 2.5 volts – 1 volt = 1.5 volts per unselected driver, instead of 4 volt per unselected driver, inside the chip.

[0013] However, because both the 5 volt power supply driver and the 2.5 volt power supply driver are coupled to the same node, e.g., output pad 104, the output voltage being driven onto the output pad by the 5 volt driver is presented at the output terminal of the 2.5 volt driver. If the 5 volt driver is driving the output pad 104 to a voltage greater than 2.5 + $V_{threshold}$ volts, it will cause reverse conduction from the 5 volt rail through output pad 104 to the 2.5 volt rail through the 2.5 volt power supply driver, causing unwanted power dissipation.

[0014] Figure 2 is a circuit diagram of an output stage 200 of an exemplary dual stage driver circuit as outlined above. The output load is represented by resistor 201. The output pad is shown at 203. The signal source, V_{IN}, is applied at the input of operational amplifier 205, the output of which is provided to a demultiplexer 207. The demultiplexer 207 provides the output of the operational amplifier 205 to either the 5 volt driver circuit 201a or the 2.5 volt driver circuit 201b.

[0015] The 5 volt driver circuit 201a is largely identical to the 5 volt driver

circuit shown in Figure 1, except for the addition of transistor M3 and demultiplexer 207 to select or deselect the 5 volt driver circuit 201a depending on the state of the select/deselect signal 209. Specifically, the 5 volt driver is selected/deselected by a SELECT1 signal 209 that controls both the demultiplexer 207 and transistor M3. Transistor M3 is a PMOS switch transistor with its source and drain coupled between the 5 volt rail and the gates of transistors M1 and M2. The 5 volt driver 201a is selected when SELECT1 goes high to 5 volts. This causes the demultiplexer 207 to send the output of the operational amplifier 205 to the 5 volt driver circuit 201a through demultiplexer output terminal 1. The SELECT1 control signal going high also turns off select transistor M3 so that the inputs to the gates of the current mirror transistors M1 and M2 are driven solely by the amplified V_{IN} signal, whereby the current through the current flow terminals of transistor M2 is controlled by V_{IN}.

[0016] To deselect the 5 volt driver 201a (i.e., the 2.5 volt driver 201b is selected), SELECT1 goes low to 1.7 volts, thus, turning transistor M3 on. This ties node 211 at the gates of the current mirror transistors M1 and M2 to the 5 volt rail through transistor M3, thus turning off transistor M2 (its source and gate are essentially tied together through transistor M3 in this state) so that it does not driver a current out to the load through M4.

[0017] In addition, a diode clamp M5 has been added to protect M2 from potentially breaking down when the 5 volt driver 201a is deselected. Specifically, node 213 between the drain of transistor M2 and the source of transistor M4 would float if not for the diode clamp M5 and could float to a voltage that could

cause Vds breakdown of transistor M2. M5 is an NMOS transistor with its source and gate tied to its tub (i.e., the p-doped well in the substrate within which an NMOS transistor is typically fabricated) and to a bias voltage V_{BIAS}. This configuration permits transistor M5 to operate as a diode from the drain terminal to the tub, thus preventing node 213 from floating when transistor M2 is off.

[0018] All of the PMOS transistors have their tubs coupled to the 5 volt rail.

[0019] With respect to the 2.5 volt driver circuit 201b, transistor M7 has its current flow terminals coupled between the 2.5 volt rail 215 and the output pad 203. Transistors M6 and M7 form a current mirror. Specifically, transistor M6 has its current flow terminals coupled between the 2.5 volt rail 215 and the demultiplexer 207. The gates of transistors M6 and M7, respectively, are coupled together at node 219, which node also is coupled to the drain of transistor M6.

[0020] Transistor M8 is the counterpart of transistor M3 of the 5 volt driver circuit 201a. Specifically, it is a PMOS transistor with its source and drain coupled between the 2.5 volt rail 215 and the gates of current mirror transistors M6 and M7. The 2.5 volt driver 201b is selected when SELECT2 signal 212 goes high to 2.5 volts and is deselected when SELECT2 goes low to 0 volts. Similarly to M3 in the 5 volt driver, when SELECT2 goes high, it causes the demultiplexer 207 to send the output of the operational amplifier 205 to the 2.5 volt driver circuit 201b through demultiplexer output terminal 2 and also turns off transistor M8 so that the inputs to the gates of the current mirror transistors M6 and M7 are driven solely by the operational amplifier.

[0021] To deselect the 2.5 volt driver, SELECT2 goes low to 0 volts, thus, turning transistor M8 on. This ties node 219 to the 2.5 volt rail 215 through transistor M8, thus turning off transistor M7 so that it does not drive a current out to the load 203.

[0022] All of the transistors M6, M7, and M8 in the 2.5 volt driver are PMOS transistors with their tubs tied to 5 volts.

[0023] Figure 3 is a schematic of the demultiplexer 207 of Figure 2. The demultiplexer input terminal 303 is coupled to the output of the operational amplifier 205. The first output terminal 305 is the output terminal to the 5 volt driver 201a and the second output terminal 307 is the output terminal to the 2.5 volt driver 201b. M20 and M21 are NMOS switch transistors with their tubs tied to circuit ground and are both controlled by the SELECT1 signal. Particularly, M20 is the switch that couples the demultiplexer input terminal to the first demultiplexer output terminal, thus coupling the operational amplifier output 205 to the 5 volt driver stage 201a. M20 has its gate directly coupled to SELECT1. M21 is the switch transistor that couples the demultiplexer input to the second demultiplexer output terminal, thus coupling the operational amplifier output 205 to the 2.5 volt driver stage 201b through a PMOS current mirror (M22, M23), a cascode transistor (M26), an NMOS current mirror (M27, M28) and a second switch transistor M30 controlled by the SELECT2 control signal.

[0024] More particularly, M21 has its gate coupled to SELECT1 through an inverter 309, which switches between 5 volts and 1.7 volts logic levels. SELECT1 also is coupled through inverter 309 to the gate of transistor M24.

M24 is a switch that turns transistors M22 and M23 off when SELECT1 is low (i.e., the 5 volt driver stage is unselected). Transistors M22 and M23 form a PMOS current mirror and M26 is a cascode device for the mirror. Cascode transistor M26 is protected by NMOS diode clamp M25 having its gate, source, and tub tied together and coupled to a bias voltage $V_{BIAS.}$ Transistors M27 and M28 form an NMOS current mirror with the transistors having their source terminals coupled to their tubs. Transistor M30 is a NMOS switch controlled by the SELECT2 signal. M30 is protected by PMOS diode clamp M29 having its gate, source and tub tied together and coupled to SELECT2. As previously noted, SELECT1 and SELECT2 are complements of each other, with SELECT1 switching between 1.7 volts and 5 volts and SELECT2 switching between 0 volts and 2.5 volts.

[0025] When SELECT1 is high (5 volts) and SELECT2 is low (0 volts), M20 is on and M21 is off such that the multiplexer input is coupled through M20 through the first multiplexer output terminal to the 5 volt driver stage and the second multiplexer output terminal is off (i.e., M30 is off). When SELECT1 is low (1.7 volts) and SELECT2 is high (2.5 volts), M20 is off and M21 is on such that the multiplexer input is instead coupled to the second multiplexer output terminal through the PMOS current mirror (M22, M23), cascode transistor M26, NMOS current mirror (M27, M28), and the current flow terminals of switch transistor M30. M30 is on by virtue of SELECT2 being high.

[0026] Although the circuit shown in Figures considerably reduces power dissipation on chip relative to the circuit shown in Figure 1, it still suffers from the drawback of reverse conduction. For instance, when the 5 volt driver is selected, depending on V_{IN}, the 5 volt driver stage 201a will drive the output pad to somewhere between 0 and about 4.5 volts. The drain of transistor M7 in the 2.5 volt driver stage 201b is coupled to the output pad 207. When the 5 volt driver stage 201a is on and the 2.5 volt driver stage 201b is off, transistor M7 will remain off as long as the voltage driven onto the output pad 207 (which is coupled directly to the drain terminal of output transistor M7) remains below about 3.2 volts, i.e., 2.5 volts plus the threshold voltage (about 0.7 volts) of transistor M7.

[0027] However, when the 5 volt driver stage 201a applies a voltage at the output pad 207 greater than 3.2 volts, that voltage on the drain terminal of transistor M7, which will cause transistor M7 to conduct in the reverse direction as illustrated by arrow 206. This is a source of unwanted power dissipation in the circuit.

[0028] Figure 4 is a circuit diagram of a modified output stage 400 for a dual driver circuit in accordance with the present invention. This circuit prevents reverse conduction in the output stage 401b of the lower voltage (e.g., 2.5 volt) driver circuit. Relative to the circuit shown in Figures 2 and 3, the following components have been added. Cascode protection transistor M9 has been added between the drain of output transistor M7 and the output pad 203. Particularly, the source of cascode protection transistor M9 is coupled to the

drain of output transistor M7 and the drain of transistor M9 is coupled to the output pad 203. In addition, transistor M10 has been added as a diode clamp for transistor M9. Its source and gate are tied together and coupled to the tub of transistor M10. This node is further coupled to the gate of cascode protection transistor M3 and the output of a comparator 405 (described below). Its drain is coupled to the source of protection transistor M9 at the node between the source terminal of transistor M9 and the drain terminal of output transistor M7. Transistor M10 is a diode clamp similar to transistor M5 in the 5 volt driver circuit 201a and will be explained in further detail below.

[0029] Other changes include that the source of switch transistor M8 has been uncoupled from the 2.5 volt rail 215 and coupled to a 4 volt rail 403. Likewise, logic levels for the select control signal to the gate of transistor M8 and the demultiplexer are changed to 1 volt to turn the 2.5 volt driver off and 4 volts to turn it on, instead of 0 and 2.5 volts, respectively. Accordingly, in Figure 4, the SELECT2 control signal of Figures 2 and 3 are replaced with a SELECT3 control signal 408 to reflect the changes in voltage levels. SELECT3 is still the complement of SELECT1.

[0030] Finally, a comparator 405 has been added. The output of comparator 405 is coupled to the node 413 at the junction of the gate of transistor M9, the gate, source and the tub of transistor M10. The non-inverting input of comparator 405 is coupled to the node 407 joining the drain terminal of transistor M9 to the output pad 203. The inverting input of the comparator 405 is

coupled to a 2.5 voltage reference. The comparator output voltage levels are 1 volt and 4 volts, respectively.

[0031] The high voltage driver (e.g., the 5 volt driver) 201a and the multiplexer 207 are essentially unchanged.

[0032] In operation, when the 5 Volt driver 201a is off and the 2.5 Volt driver 401b is on, the voltage range at the output pad 203 will be about 0-1.5 volts. Since the output pad 203 is coupled to the non-inverting input of the comparator 405, the comparator 405 will apply 1 volt to the gate of cascode protection transistor M9 whenever the 2.5 volt driver 201b is on and the 5 volt driver 201a is off. This turns on cascode protection transistor M9 so that the output of transistor M7 will be passed through the current flow terminals (source and drain) of transistor M9 to the output pad 203, providing normal operation generally as previously described. However, when the 5 volt driver is on and the 2.5 volt driver is off and the voltage placed on the output pad 203 exceeds the 2.5 volts threshold of the comparator, the comparator output will switch to 4 volts. This voltage applied at the gate of transistor M9 will turn off the transistor. The voltage at the drain of transistor M9 is the voltage on the output pad 203, which will be somewhere between 0 volts and the 4.5 volt maximum drive voltage of the 5 volt driver. Since the maximum possible voltage at the drain of transistor M9 is 4.5 volts, which is only 0.5 volts higher than the 4 volts applied at the gate of transistor M9, M9 cannot turn on (because the threshold voltage of transistor M3 is at least 0.5 volts, and usually about 0.7 volts). Accordingly, reverse

conduction through output transistor M7 is not possible because the path from the output pad 203 to output transistor M7 is open circuited by M9.

[0033] The diode clamp transistor M10 is included to prevent node 411 from floating when the protection circuit is operating and no current is flowing through node 411 (i.e., when M9 is turned off). If not for the diode clamp M10, node 411 could float to any voltage (even to 0 volts) without current flowing, which could lead to gate breakdown of M7. Particularly, the Vds and gate oxide breakdown voltage for transistors fabricated by 3.5 volts CMOS fabrication techniques is 3.5 volts. Thus, if the gate of M9 is at 4 volts and node 411 floats to 0 volts, gate oxide breakdown will occur in output transistor M7. Thus, the diode clamp M10 is coupled between the gate and the source of the protection transistor M9 to keep the node 411 between the protection transistor M9 and the output transistor M10 from floating when no current is flowing.

[0034] As noted above, the bias voltages applied to the source of switch transistor M8 should be 4 volts instead of 2.5 volts (as it was in the prior art circuit of Fig. 2.) Furthermore, the SELECT3 logic levels applied at the gate of switch transistor M8 should be 1 volt to turn the 2.5 volt driver off and 4 volts to turn it on, instead of 0 volts and 2.5 volts, respectively.

[0035] Specifically, with diode clamp M10 in place, when transistor M9 is off with no current flowing, node 411 will be at 4 volts. Therefore, in order to keep output transistor M7 off when transistor M9 is off, the gate voltage of M7 also must be maintained at about 4 volts. More broadly, the bias voltage at the source of M8 should be no further away from the 4 volts supplied from the

comparator output than one threshold voltage of M7. This is why the source and gate of transistor M8 is coupled to a 4 volt rail (rather than the 2.5 volt rail as in prior art Fig. 2). Thus, in turn, the SELECT3 voltage applied at the gate of transistor M8 to turn it on should switch between 4 volts and 1 volt, rather than 2.5 volts and 0 volts, in order to prevent the voltage differential between the source and gate of PMOS transistor M8 from exceeding the junction breakdown voltage of transistor M8 when SELECT3 is unselected (i.e., when SELECT3 is low).

[0036] In the circuit of Figure 4, all of the PMOS transistors have their tubs tied to the 5 volt rail.

[0037] This protection scheme comprises minimal additional circuitry and prevents unnecessary power dissipation on the chip when the higher voltage driver is on and the lower voltage driver is off.

[0038] Having thus described one particular embodiment of the invention, various alterations, modifications, and improvements will readily occur to those skilled in the art. Such alterations, modifications and improvements as are made obvious by this disclosure are intended to be part of this description though not expressly stated herein, and are intended to be within the spirit and scope of the invention. Accordingly, the foregoing description is by way of example only, and not limiting. The invention is limited only as defined in the following claims and equivalents thereto.